## REMARKS

Claims 1-30 are pending in the application. Claims 1-5, 7, 11, 17, 18, 21 and 24-26 have been amended. No new matter has been added. Applicants respectfully request reconsideration of the rejections set forth in the Office Action dated September 2, 2004 in light of the preceding amendments and the following remarks.

Applicants thank the Examiner for the courtesy extended during the telephonic interview with Applicants' representative on December 2, 2004. During this interview, the rejections, references and on-chip memory were discussed.

The present invention increases processing speed for motion compensation. A reference sub-region needed for motion compensation, as identified by motion information, is obtained in advance of motion compensation. The reference sub-region is stored in on-chip memory prior to motion compensation. Obtaining and storing multiple reference sub-regions in advance of motion compensation in this manner allows motion compensation to proceed without continuous data access delays.

The claims have been amended to clarify the present invention. Claim 1, for example, has been amended and now recites "storing the reference sub-region identified by the motion information in an on-chip memory before performing motion compensation using the set of motion vectors". No new matter has been added. Support for this amendment can be found throughout the Specification, and in particular on page 8, lines 18-30 (see FIG. 2), and page 10, line 27 to page 13, line 27, for example. Page 8, lines 23-24 specifically state that the on-chip memory 60 forms part of processor 52 and may include a non-volatile RAM and/or ROM.

### Rejections Under 35 U.S.C. §102(b)

Claims 1-24 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,812,791 ("Wasserman"). Claims 1-2, 5-13, 17-20, and 21-24 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,084,637 ("Oku"). Applicants respectfully traverse both rejections.

The claims now recite 'on-chip' memory. As one of skill in the art will appreciate, on-chip memory is a commonly used and well-known term that refers to a memory local to a

processor. FIG. 2 of the specification shows one example of on-chip memory 60 (and off-chip memory 56). In this case, a bus 58 separates off-chip memory 56 from processor 52, while memory 60 forms part of processor 52, such as non-volatile RAM and/or ROM.

Neither Wasserman or Oku teach or suggest an on-chip memory source. For Wasserman, the Office Action uses system memory 110 to teach on-chip memory (see page 3 of the Office Action dated 9/2/2004). Quite oppositely, item 150 of Wasserman in FIG. 2 is an ASIC (Application Specific Integrated Circuit), which is typically a separate chip. System memory 110 is unmistakably depicted outside the border of ASIC 150 (see FIG. 2) and thus cannot be 'on-chip'. For Oku, memory 11 is also accessed via a command bus or data bus (see fig. 1) and also cannot be 'on-chip'. Thus, both references, either alone or in combination, do not teach on-chip memory.

While Wasserman teaches a FIFO buffer, one of skill in the art will appreciate the difference between on-chip memory (e.g., a separate RAM) and a FIFO buffer. For example, a FIFO buffer is a blind and small temporary reservoir that holds data until some next data comes (no spatial or temporal control), while on-chip memory (such as a non-volatile ROM) is addressable, much larger and permits temporal control. The two are distinct from a computer architecture perspective.

The claims also recite "before motion compensation" to reflect that a sub-region needed for motion compensation is obtained in advance of motion compensation (see elements i and iv). The art of record also lacks this limitation and obtains data as motion compensation occurs and not in advance.

For at least these reasons, independent claims 1, 17, 21 and 24 are allowable.

Claim 17 also recites "storing the set of reference window sub-regions included in a reference window identified by the motion information in an on-chip memory". Neither reference discloses such a reference window or storing a reference window in an on-chip memory. For Wasserman, the Office Action dated November 12, 2003 points to fig. 8 to teach a reference window. However, this figure of Wasserman shows the organization of macroblocks and division of the macroblocks into halves (see col. 20, lines 45-49). Nowhere in the description of fig. 8 does Wasserman teach a reference window, storing the reference window, or storing the reference window in an on-chip memory. For Oku, the Office Action dated November 12, 2003 points to fig. 30 of Oku to teach a reference window. However, this diagram shows a switching operation of four kinds of memory map (see col. 26, lines 25-30). This section does not teach a reference window, storing the reference window, or on-chip memory.

Therefore, Applicants respectfully submit that Wasserman and Oku, alone or in combination, do not teach or suggest independent claims 1, 17, 21, 24 and 27 and that the independent claims are allowable.

Dependent claims 2-16, 18-20, 22-23 and 25-26 each depend directly from independent claims 1, 17 and 21 and are therefore respectfully submitted to be patentable over Wasserman and Oku for at least the reasons set forth above with respect to the independent claims. Further, the dependent claims recite additional elements which when taken in the context of the claimed invention further patentably distinguish the art of record. For example, depending claim 8 recites "wherein the time that the reference sub-region is stored in the on-chip memory before performing motion compensation using the set of motion vectors comprises an estimated time for a processor to reconstruct one macroblock". The Office Action dated November 12, 2003 points to the CPU 102 and system memory 110 of FIG. 2 of Wasserman to teach this limitation. Dependent claim 8 does not recite a processor and memory, and this estimated time limitation is not taught by the reference. For at least these reasons, dependent claim 8 is allowable.

Withdrawal of the rejections under 35 USC §102(b) is therefore respectfully requested.

Applicants believe that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Applicants hereby petition for an extension of time which may be required to maintain the pendency of this case, and any required fee for such extension or any further fee required in connection with the filing of this Response is to be charged to Deposit Account No. 50-0388 (Order No. CISCP229).

Respectfully submitted,
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Limited Recognition under 37 C.F.R.§10.9(b)

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**Expires: April 21, 2005**

Harry I. Moatz
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